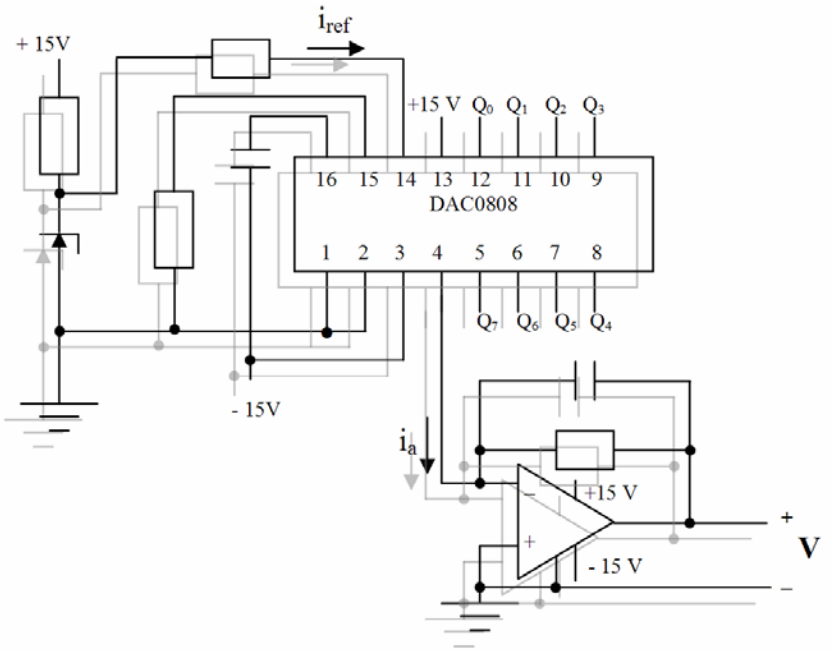
INNLEIÐANDI ELEKTRONIKKUR

Starvsstovuvenjingar

Magnus Danielsen



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INNIHALDSYVIRLIT

Fororð:
Hesar síður eru leiðbeiningar til starvsstovuvenjingar í lærugreinini ”digitalur elektronikkur”, ið er innleiðandi elektronikklærugrein í lestri til BSc í ravmagnsverkfrøði á Náttúruvísindadeildini á Fróðskaparsetri Føroya.

I. OPERATIÓNSSTYRKJARAR
STARVSTOVUVENJING

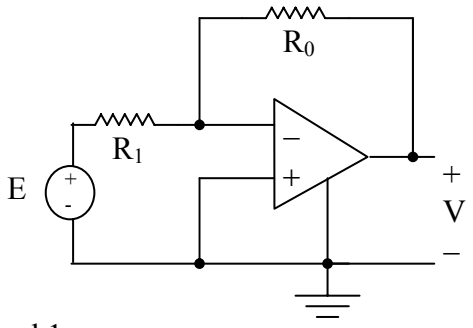
Inngangur
Í venjingini verður ein operatiónsstyrkjari settur upp í eina streymrás og royndur í tveimum ymiskum uppsetingum:

– Í fyrru uppsetingini virkar hann sum ein einfaldur styrkjari
– Í seinnu uppsetingini virkar hann sum ein summatiónsrás og leggur fleiri spenningar saman.

Uppsetingarnar skulu roynast bæði við telduforritinum PSpice og í eini uppseting av elektronisku lutunum í starvsstovuni.

Tað er týdningarmikið at fyrireika seg væl og, at **allir teir teoretisku spurningarnir eru svaraðir, áðrenn møtt verður í starvsstovuni**. Tíðin í starvsstovuni er bert 2 tímar. Stutt frágreiðing um venjingina skal verða skrivað.

1. Einfaldur styrkjari
Í myndini er ein operatiónsstyrkjarauppseting víst.



Mynd 1

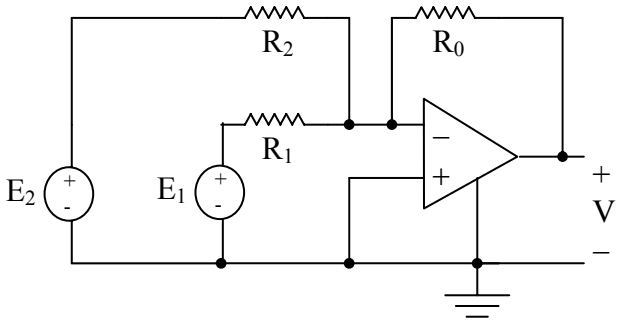
$R_1 = 0{,}5\ k\Omega$
Forsýningsspenningarnir, ið nýttir verða, eru +10 volt og –10 volt

Spurningar at svara áðrenn møtt verður í starvsstovuni:
1.1. Hvussu stórur skal R_0 vera fyri, at styrkingin A=V/E skal hava virðið –10 ?
1.2. Hvussu stór eru approksimativu metningsvirðini á útgangsspenninginum V?

Spurningar at svara við brúk av teldusimuleringsforritinum PSpice:
1.3. Ger eina uppseting av operatiónsstyrkjaranum í telduni við funnað virðinum fyri R_0 og prenta tekningina (diagrammið) til at seta í frágreiðingina.
1.4. Ger eina simulering av útgangsspenninginum sum funktión av inngangsspenninginum við –15 volt < E < +15 volt. Prenta myndina til at skjalfesta úrslitið.
1.5. Hvussu stór er styrkingin í linjurætta økinum?
1.6. Hvat virði hava metningsvirðini á útgangsspenninginum?

Spurningar at svara í starvsstovuni:
1.7. Ger eina uppseting av styrkjaranum og eina tekning (diagramm) av uppsetingini.
1.8. Máta útgangsspenningin sum funktión av inngangsspenninginum –15 volt < E < +15 volt.
1.9. Hvussu stór er styrkingin í linjurætta økinum?
1.10. Hvat stødd hava metningsvirðini á útgangsspenninginum?

2. Summatións rás



Mynd 2

Set virðini á inngangsspenningunum til
E_1 = 2 volt
E_2 = 3 volt

Set $R_0 = R_1 = R_2 = 1$ kΩ

Spurningar at svara áðrenn møtt verður í starvsstovuni:

2.1. Rokna virði á útgangsspenninginum V

Spurningar at svara við brúk av teldusimuleringsforritinum PSpice:

2.2. Ger eina uppseting av summatiónsrásini á telduni, prenta tekningina til at seta í frágreiðingina.
2.3. Ger eina simulering av rásini og avger virðið á útgangsspenninginum V.
2.4. Hvussu stórur er feilurin í %.

Spurningar at svara í starvsstovuni:

2.5. Ger eina uppseting av styrkjaranum og eina tekning (diagramm) av uppsetingini.
2.6. Máta útgangsspenningin sum funktión av inngangsspenninginum
2.7. Hvussu stórur er feilurin í %.
2.8. Hvussu kanst tú útbyggja uppsetingina soleiðis, at forteknið á V verður rætt í einari summatiónsprosess. Set uppsetingina upp og royn hana, um tíðin loyvir tí.

II. RC - RÁS
STARVSTOVUVENJING

Inngangur
Venjingin skal vísa, hvussu ein kondensator í eini streymrás, sum annars bert inniheldur spenningsgerða og mótstøður, háttar sær.

Í venjingini verður ein kondensator settur upp í eina streymrás og royndur í tveimum ymiskum førum:
- Í fyrra føri verður spennigsgerði, ið kann skifta millum tvey spenningsvirði settur til, og spenningurin yvir kondensatorin, og streymurin gjøgnum eina av mótstøðunum í rásini verður mátaður.
- Í seinna føri verður pulsgerði við føstum formi gjørdur, har trin-spenningur frá spenningsgerða er brúktur til at avgera, nær ein fýrkantaður spenningspulsur verður gjørdur. Hetta verður gjørt við hjálp av kombinatoriskari streymrás, har umframt IC rásir eisini mótstøða og kondensator innganga til at avgera pulslongdina. Skiftið millum lágan og høgan útgangsspenning er ikki skarpt við vanligum IC komponentum. Tí er betur, at IC rásir við Schmitt triggara inngangi verða nýttir.

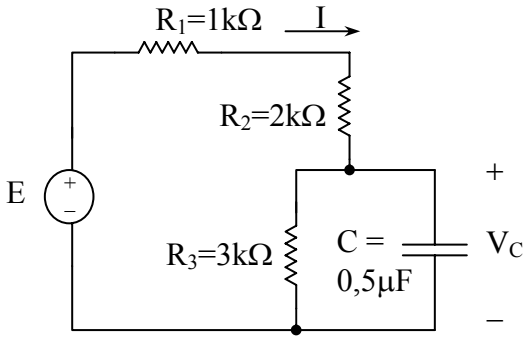
Uppsetingarnar skulu roynast bæði við telduforritinum PSpice og í eini uppseting av elektronisku lutunum í starvsstovuni.

Tað er týdningarmikið at fyrireika seg væl og, at **allir teoretisku spurningarnir eru svaraðir, áðrenn møtt verður í starvsstovuni**. Tíðin í starvsstovuni er bert 2 tímar. Stutt frágreiðing um venjingina skal verða skrivað.

1. RC-rás við fýrkants spenningsgerða
Í myndini er ein RC-rás vist. E er spenningsgerði, ið gevur ein periodiskan fýrkantspenning frá sær

$$E = \begin{cases} 5V & 0 \le t < \dfrac{T}{2} \\ 0V & \dfrac{T}{2} \le t < T \end{cases}$$

har periodan $T >> \tau$, ið er tíðarkonstanturin fyri rásina. Hetta merkir, at spenningar og streymar kunnu verða útroknaðir frá treytini, at E er ein trinspenningur.



Spurningar at svara áðrenn møtt verður í starvsstovuni:

1.1. Rokna virðið á tíðarkonstantinum τ.

1.2. Finn virðið á $V_C(0_-)$, $V_C(0_+)$ og $V_C(\infty)$ umframt $I(0_-)$, $I(0_+)$ og $I(\infty)$ í tí føri, at E skiftir frá 0V til 5V.

1.3. Tekna $V_C(t)$ og I(t) sum funktión av tíðini t.
1.4. Svara spurningunum 1.1 til 1.3 í tí føri, at E skiftir frá 5V til 0V.

Spurningar at svara við brúk av teldusimuleringsforritinum PSPICE:

1.5. Ger eina uppseting av rásini í telduni við givnum mótstøðum og kondensatorvirði, og har T=5ms.
1.6. Ger simulering av $V_C(t)$ og I(t).

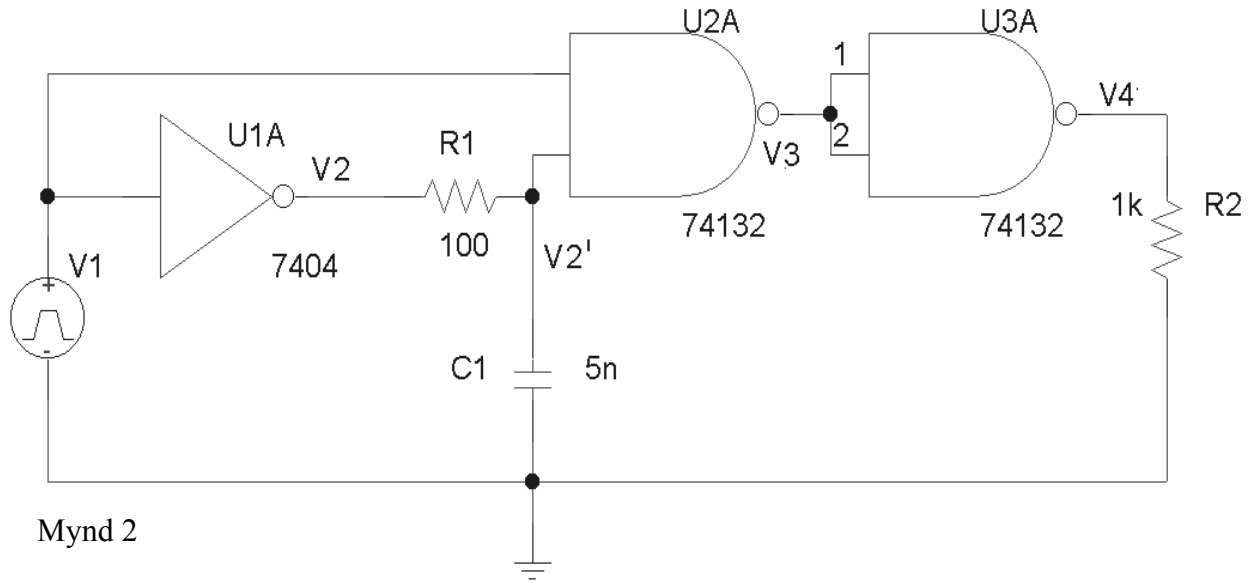
Spurningar at svara í starvsstovuni:

1.7. Ger eina uppseting av RC-rásini og eina tekning (diagramm) av uppsetingini. (Ansa eftir, at spenningsgerðin hevur eina innaru mótstøðu, sum skal vera partur av mótstøðuni R_1 soleiðis, at samlaða mótstøðan R_1 = 1 kΩ)
1.8. Máta spenningin $V_C(t)$ og streymin I(t) sum funktión av tíðini t við einum oscilloscopi. I(t) kann verða mátaður t.d. við at máta spenningin yvir R_2 (verður mátaður við at máta potentialið á báðum endum á R_2 við tveimum kanalum á oscilloscopinum og draga frá).
1.9. Samanber við tey útroknaðu og simuleraðu úrslitini.

2. RC-rás til gerð av pulsgerða, ið gevur puls við føstum formi.

Í streymrásini í mynd 2 er V1 ein pulsspenningsgerði, sum gevur invertaranum U1A ein spenning, sum broytist frá V1 = 0 volt til V1 = 4 volt. Útgangurin V2 broytist tá tilsvarandi frá o.u. 4 V til 0 V. U2A, sum er ein NAND gate, fær annan inngangsspenningin beinleiðis frá V1, og hin spenningin V_2' umvegis R1 og C1 frá V2. Útgangurin V3 verður so inverteraður í invertaranum U3A soleiðis, at endaligi útgangsspenningurin V4 gevur tann ynskta pulsin. Her er U3A, sum í veruleikanum er ein NAND-gate, brúktur sum invertari við at samankobla inngangirnar (vís hví hann virkar so!).

Tað eigur at verða lagt merki til, at NAND-gaturnar av slagnum 74132 hava Schmitt triggara í innganginum til tess at fáa ein meira fullkomnan fýrkantpuls á útganginum. Aðrar NAND-gatur eru eisini, t.d. 7400, ið ongan Schmitt triggara hava, men verða ikki brúktar her.



Mynd 2

Spurningar at svara heima

2.1. Ger frágreiðing um, hvussu rásin virkar við t.d. at skitsera V_1, V_2, V_2', V_3 og V_4.
2.2. Rokna virðið á tíðarkonstantinum τ.
2.3. Finn virði á V'(0_-), V'(0_+) og V'(∞), og formulin fyri V'(t). Ger tekning av V'(t).

Invertarin U1A verður her í teoretisku útrokningunum roknaður at hava útgangsvirðini o.u. 3,8 volt í høgari støðu, og 0,2 volt í lágari støðu. Tilsvarandi er lágur skiftispenningur á inngnginum á U2A 0,8 volt, og høgur skiftispenningur 2,4 volt.

2.4. Rokna út breiddina á fýrkantspulsinum á útganginum. (Set skifti inngangsspenningin í U2A til 0,8 V.)

Spurningar at svara við PSPICE

2.5. Ger eina uppseting av rásini við simuleringsforritinum í telduni við teimum givnu mótstøðunum og kondensatorinum. Prenta rásina.
2.6. Ger simulering av V1, V2, V2', V3 og V4 sum funktión av tíðini.

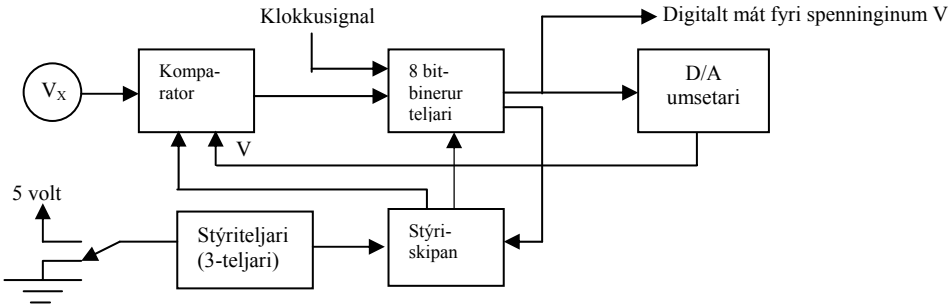
Spurningar at svara í starvsstovuni:

2.7. Ger eina uppseting av RC-rásini og eina tekning (diagramm) av uppsetingini.
2.8. Máta spenningarnar V1, V2, V2', V3 og V4 sum funktión av tíðini við oscilloscopinum. Ger tekning av hesum og finn pulsbreiddina á V4.
2.9. Samanber við tær útroknaðu og simuleraðu úrslitini
2.10. Hví gevur Schmitt triggarin ein meira fulkomnan puls á útganginum?

III. EINFALT DIGITALVOLTMETUR
STARVSTOVUVENJING

1. Inngangur
Í venjingini verða prinsippini fyri uppbygging og virkihátti av einum digitalvoltmetri kannað og greind. Digitalvoltmetrið er uppbygt av undireindum. *Týdningarmikið er, at hvør eindin sær fyrst verður uppbygd, kannað og skjalprógvað.* Síðan verða tær bundnar saman til eina samanhangandi skipan, ið myndar tað samlaða digitalvoltmetr-ið. Tað er ikki skilagott og verður rátt frá at seta alla uppsetingina upp beinanvegin uttan at kanna hvørja undireind sær. Yvirlitið yvir rásina verður lættari mist við at gera tað.

2. Einføld digitalvoltmeturskipan.
Digitalvoltmetrið er ein skipan, ið mátar ein spenning og umger mátiúrslitið til eitt tal, sum í hesi roynd er eitt binert tal við 8 bittum. Hátturin, digitalvoltmetrið virkar uppá er í stuttum hesin. Ein stýristreymrás (stýriskipan) fær ein elektroniskan bineran teljara at telja upp til eitt talvirði, sum svarar til tann spenningin V_X, ið vit skulu máta. Tann bineri 8 bit teljarin telur klokkusignalpulsar frá nul og upp til eitt tal, har hann verður steðgaður av einum signali frá komparatorinum. Komparatorin ger sítt



Mynd 2.1 Yvirlitsrás.

útgangssignal við at samanbera spenningin V_X við eitt analogt spenningssignal V, sum D/A umsetarin ger burtur úr digitala útgangssignalinum frá teljaranum. Tá hetta spenningssignalið V fer upp um V_X skal komparatorin steðga binera teljaranum. Teljara-virðið, ið bineri teljarin tá hevur talt upp til, er eitt digitalt mát fyri spenninginum V_X.

Tað digitala voltmetrið verður stýrt av eini stýriskipan til at vera í einum av trimum ymiskum støðum:

Støða 1: voltmetrið er nullstillað
Støða 2: voltmetrið mátar ein spenning
Støða 3: voltmetrið verður roynt, um tað er ført fyri at máta upp til fullan spenning, og um "displayið" (her ljósdiodur) er í lagi.

Stýriskipanin fær eitt digitalt signal svarandi til hesar støður frá einum teljara, ið kann telja upp til 3 (trýteljara). Trýteljarin verður hin vegin stillaður við einum trýst-umskiftara, ið gevur honum hondstýrdar spenningspulsar sum inngangssignal.

Fyrsta trýst gevur 1. støðu, annað trýst gevur 2. støðu, og triðja trýst gevur 3.støðu, og o verður byrjað av nýggjum. Umframt signalið frá trýteljaranum, fær kontrolskipanin eisini eitt signal frá útganginum av binera teljaranum.Hetta signalið sigur frá, nær bineri teljarin hevur talt upp til maksimum.

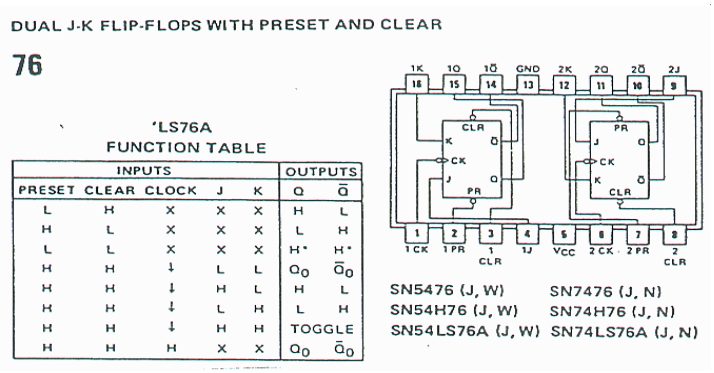
Tað er endamálið við hesi venjing at byggja upp tær ymsu lutskipaninar hvør sær og royna tær. Síðan skulu tær bindast saman til eitt samlað digitalvoltmetur, ið her hevur binera útlesing til 8 ljósdiodur sum detektorar, eina til hvørt einstakt bit.
Venjingin er skipað í:

1. ein fyrireikingarpart, ið snýr seg um at seta seg inn í tað neyðturvuliga lærubókatilfarið til at kunna skilja og loysa spurningarnar í hesi venjingini (er umfatað av tí sum higartil er gjøgnumgingið),
2. nakrar teoretiskar spurningar í samband við uppbygging av skipanini og *skulu verða svaraðir áðrenn, møtt verður upp í starvsstovuni,*
3. sjálva starvsstovuvenjingina, sum snýr seg um at uppbyggja skipanina, fáa hana at virka, gera neyðugar mátingar og avlesingar. *Hvør lutskipan sær skal uppbyggjast, roynast og skjalprógvast áðrenn, tær verða bundnar saman til eina heildarskipan.*
4. og dokumentera bæði uppbygging og úrslit, og skriva eina samanhangandi frágreiðing um úrslitini.

Viðmerking: tak ikki lutskipaninar sundur aftur beinanvegin, tá tær eru royndar. Tær skulu, tá tær allar eru fingnar at virka, bindast saman í eina samlaða digitalvoltmetur-skipan.

2.1 3-teljari til funktiónsskiftara. Teljisekvensur 00 01 10 00 .....

Tveir MS-JK flip-flop, báðir integreraðir í ein "chip" 74LS76 , hvørs datablað uppgevur sannleikatalvuna í mynd 2.1.1, verða brúktir til henda 3-teljaran. Tveir flip-flop'ar kunnu, tá teir eru hóskandi bundnir saman telja til í mesta lagi $2^2 = 4$ ymsar støður. Í hesi royndini eru bert 3 støður ynsktar, har Q-útgangirnir hava virðini 00 01 10, meðan 11 ikki skal fyrikoma.


DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

76

'LS76A

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

SN5476 (J, W) SN7476 (J, N)
SN54H76 (J, W) SN74H76 (J, N)
SN54LS76A (J, W) SN74LS76A (J, N)

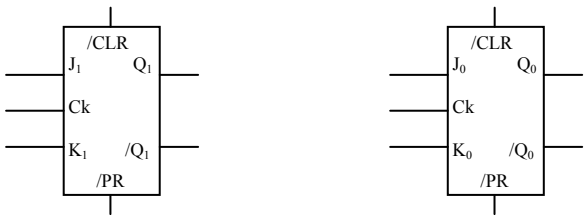
Mynd 2.1.1 MS-JK flip-flop 74LS76, partur av datablaði.

At svara, áðrenn møtt verður í starvstovuni:
Spurningur 1: Konstruera umvendu sannleikatalvuna, talva 1, hjá eini MS-JK flip-flop rás við at seta "0", "1" og "don't care" støður í talvuna.

Spurningur 2: Útfyll talvuna 2 og tíðarfarmyndina mynd 2.1.3.

Spurningur 3: Tekna á hesum grundarlagi eina streymrás (diagramm) fyri 3-teljaran, t.e. samanbind MS-JK flip-flop rásirnar í mynd 2.1.2 við leiðarum og møguligum (um neyðugt) kombinatoriskum IC rásum (AND, OR og NOT).

At svara í starvstovuni:
Spurningur 4: Set teljararásina upp í starvsstovuni og royn teljaran við at geva honum (klokku-) pulsir inn og hyggja at Q_1 Q_0 við ljósdiodum ella oscilloscopinum.



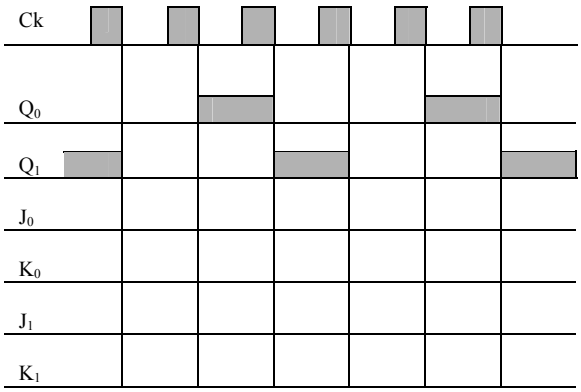
Mynd 2.1.2 Tveir MS-JK flip-flop'ar
at binda saman til ein trýteljara.

Q(n)	Q(n+1)	J(n)	K(n)
0	0		
0	1		
1	0		
1	1		

Talva 1.Umvend sannleikatalva
(til at fylla út)

Ck(n)	Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	0				
1	0	1				
2	1	0				
3	0	0				
4	0	1				
5	1	0				

Talva 2 Sannleikatalva fyri trýteljara.
(til at fylla út)



Mynd 2.1.3 Tíðarskifti fyri trýteljara
(til at fylla út)

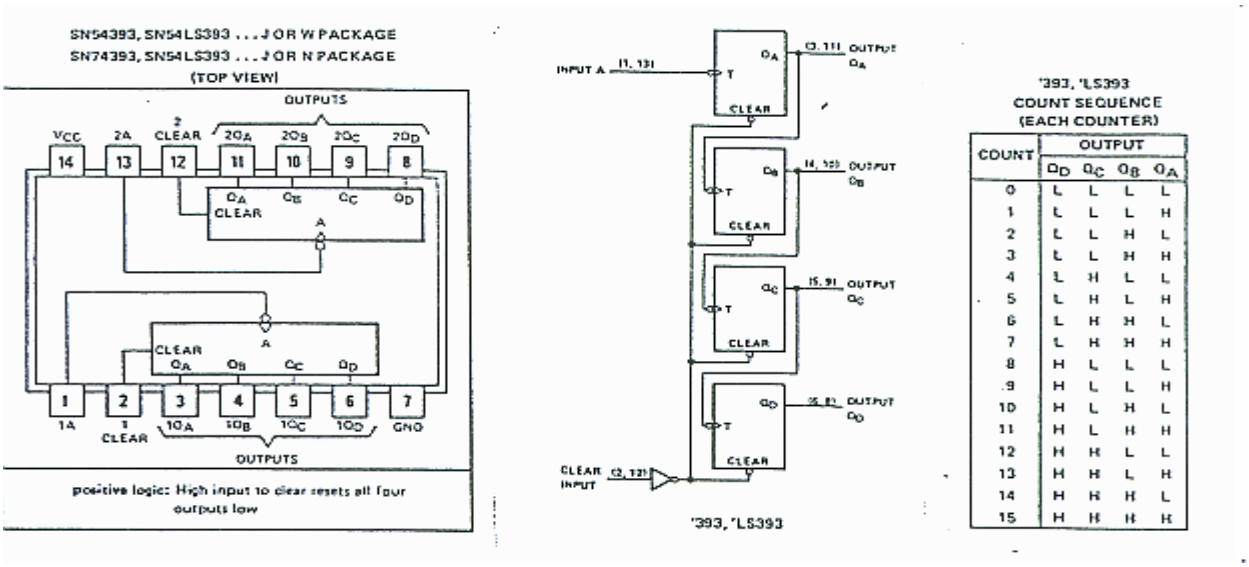
2.2 Binerur 8 bit teljari

Ein 8 bit binerur teljari (256-teljari) verður uppbygdur við brúk av einari 74LS393 IC-teljararás, sum víst er í Mynd 2.2.1. Í 74LS393–rásini eru tveir 4 bit teljarar.

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 5: Tekna eina streymrás (diagramm) fyri 256-teljaran, t.e. samanbind teljararásirnar í mynd 2.2.1 við leiðarum, og vís, hvussu spenningar verða settir til, og hvussu útlesing fer fram.

At svara í starvsstovuni:

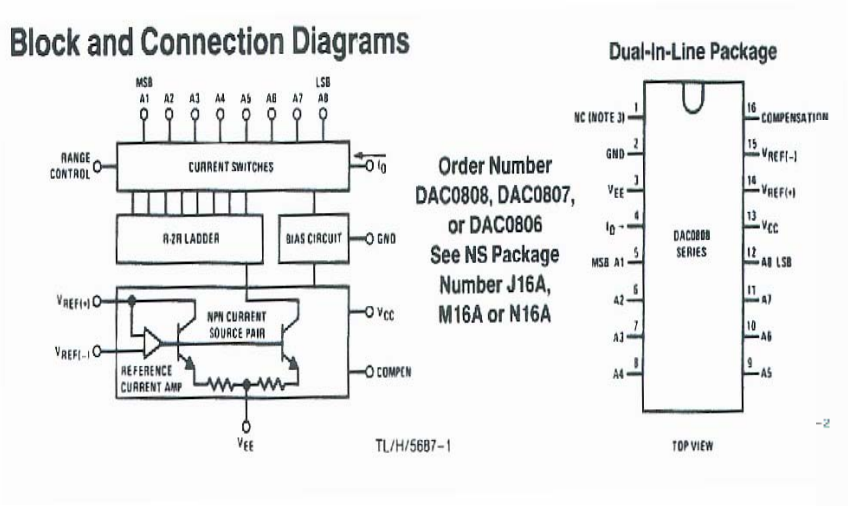
Spurningur 6: Set 256-teljararásina upp í starvsstovuni og royn teljaran við at geva honum (klokku-) pulsir inn og hyggja at útgangsbittunum við ljósdiodum og oscilloscopinum.



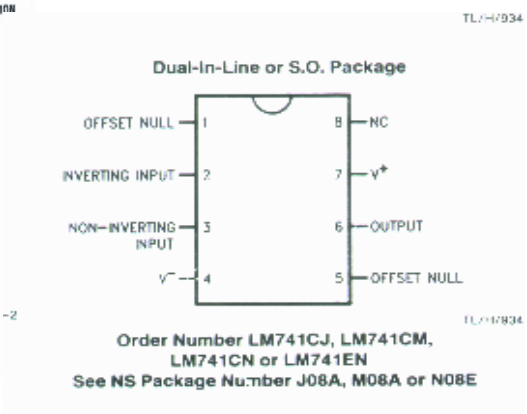
Mynd 2.2.1 Tveir binerir teljarar í einari IC-rás 74LS393. Partur av datablaði.

2.3 Digital – analog umsetari

Í uppbyggingini av digitalvoltmetrinum, sum í veruleikanum er ein analog-digital umsetari, verður ein digital-analog umsetari brúktur. Hesin verður konstrueraður við brúk av eini digital-analog umsetara IC-rás DAC0808 (8 bit), ið gevur ein streym i_a á útganginum, ið er proportionalur við digitalvirðið á teimum 8 innkomandi bittunum, og einum operatións-styrkjara, t.d. LM741 (u741), ið ger ein útgangsspenning V, sum er proportionalur við hendan streymin. Datablað fyri DAC0808 er partvís víst í mynd 2.3.1, og fyri u741 í mynd 2.3.2.



Mynd 2.3.1 D/A umsetari DAC0808.
Partur av datablaði.



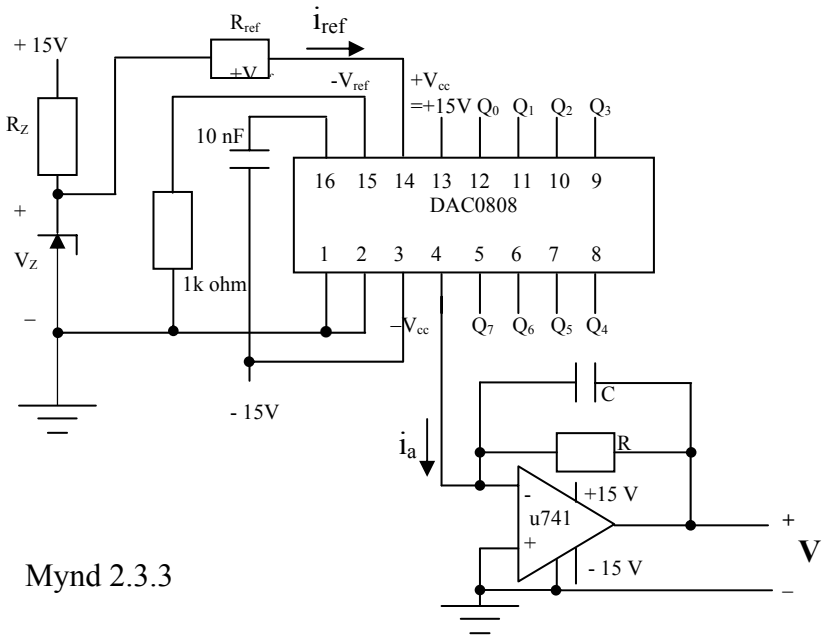
Mynd 2.3.2 Operatiónsstyrkjari LM741 (u741).
Partur av datablaði.

Í mynd 2.3.3 er ein streymrás sett upp fyri ein digital-analog umsetara, sum hevur spenningin V á útganginum, ið er proportionalur við streymin i_a og harvið eisini við binera talið $0.Q_7\ Q_6\ Q_5\ Q_4\ Q_3\ Q_2\ Q_1\ Q_0$. (Her eru bittini nevnd Q, meðan í datablaðnum stendur A.)

Fyri DAC0808-rásina er givið, at streymurin

$$i_a = i_r\ [\ ½\ Q_7 + (½)^2\ Q_6 + (½)^3\ Q_5 + (½)^4\ Q_4 + (½)^5 Q_3 + (½)^6\ Q_2 + (½)^7\ Q_1 + (½)^8 Q_0],$$

har i_r er referensustreymurin sum kemur inn í refensuinngangin (bein 14) á DAC0808.



Mynd 2.3.3

Referensuinngangurin "V_{ref} " (bein 14) hevur ein sera lítlan inngangsmótstand, ella vit kunnu siga, at hann er "virtuelt nul". Hetta merkir, at I_{ref} verður avgjørdur av tí ytru streymrásini, ið er samansett av eini zenerdiodu, ið skapar ein næstan konstantan spenning, og tveimum mótstøðum R_Z og R_{ref}.

Operatiónsstyrkjarin virkar sum ein transresistanskoblaður styrkjari, ið ger ein spenning á útganginum V, sum er proportionalur við I_a . Kondensatorarnir 10 nF og C hava onga beinleiðis ávirkan á úrslitið og eru við í rásini bert fyri at sleppa undan sjálvsvingi í rásini. Tí er valið av teimum eisini ókritiskt.

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 7: Referensustreymurin I_{ref} =2 mA er ein passandi støddsambært datablaðnum. Zenerspenningurin V_Z = 6 volt, og streymurin gjøgnum zenerdioduna er settur at vera 10 I_Z fyri at stabilisera spenningin. Hvussu stórir eru R_Z og R_{ref} .

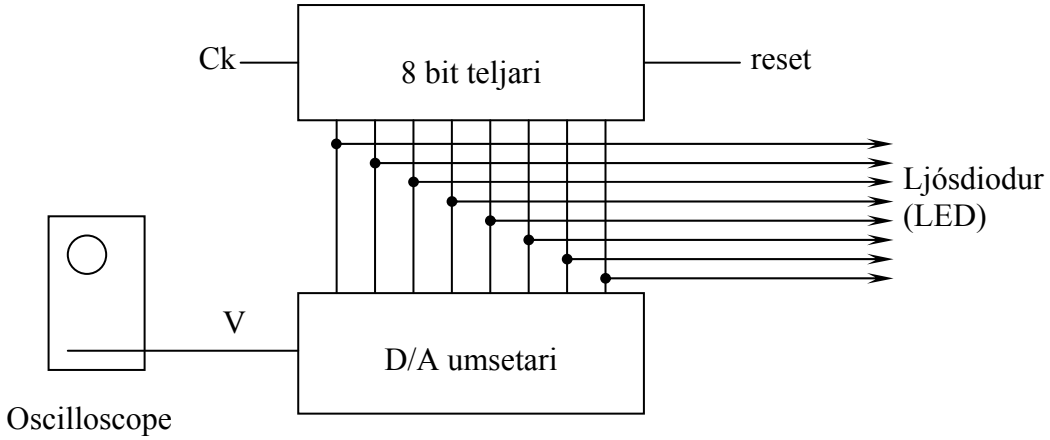
Spurningur 8: Hvussu stór er mótstøðan R fyri, at útgangsspenningurin í mesta lagi skal vera 10 volt.

At svara í starvsstovuni:
Spurningur 9: Set digital-analog umsetaran upp (tað er møguligt, at zenerspenningurin ikke er neyvt 6 volt. Í so fall skal R-virðið, sum gevur júst 10 volt út, svarandi til aktuella

zenerspenningin finnast í starvsstovuni, meðan R_Z og R_{ref} hava óbroytt virði). Royn við givnum valdum bit virðum fyri Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0 á inngangunum um tilsvarandi spenningur V er á útganginum á D/A umsetaranum.

2.4 Rampu-trapputrinsspenningsgerði, samansettur av teljara og D/A umsetara

Vit kunnu nú sum víst í mynd 2.4.1 seta útgangsbittini á teljaranum til tilsvarandi inngangsbit í D-A umseraranum og lata teljanan telja frá 0 til 255. Útgangssignalið verður tá ein vaksandi spenningur, sum í trapputrinum veksur frá 0 til 10 volt.



Mynd 2.4.1

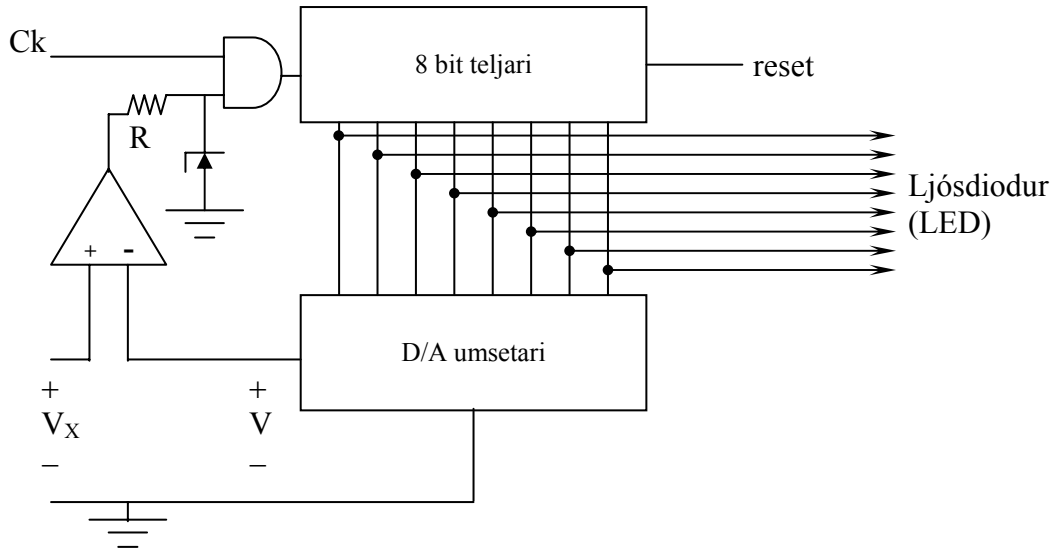
At svara í starvsstovuni:

Spurningur 10: Set rampu-trappuspenningsgerðan saman av 8-bit teljaranum og D/A umsetaranum. Máta V sum funktión av tíðini við oscilloscopinum. Tekna úrslitið upp.

Spurningur 11: Set eina talvu upp, har spenningurin verður uppgivin fyri hvørt av digitalvirðunum á Q-útgongdunum (øll 256 virðini eru ikki neyðug, men uppgev 10 tey fyrstu og 5 tey seinastu virðini). Máta støddina av trapputrinunum, og samanber við, hvat tað teoretiskt skal vera.

2.5 Spenningssamanberari (comparator) og digitalvoltmetur uttan funktiónsskiftara

Vit hava higartil sæð, hvussu ein teljari fær ein spenning at vaksa frá nul til 10 volt. Vit skulu nú gera tann partin av eini stýriskipan, sum ger samlaðu skipanina soleiðis skikkaða, at hon fær teljarin at steðga, tá útgangsspenningurin V er komin upp til virði hjá tí ókenda spenninginum V_X , ið endamálið við einum digitalvoltmetri er at máta. Hetta merkir, at útgangsvirði av tí 8 bit binera talinum, sum teljarin vísir júst er eitt mát fyri tí ókenda spenninginum V_X. Hetta verður gjørt við einum komparatori, ið verður bygdur upp sum myndin 2.5.1 vísur við einum operatiónsstyrkjara einari Zenerdiodu og einari "AND-gate".



Mynd 2.5.1

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 12: Hvussu stórur skal zenerspenningurin hjá dioduni vera. Áset eitt hóskandi virði fyri mótstøðuna R í komparatorinum.

At svara í starvsstovuni:
Spurningur 13: Set komparatoruppsetingina upp í starvsstovuni og royn við ymsum spenningum á inngonginum um tilsvarandi biner digitalvirði koma á Q-útgangirnar.

2.6 Funktiónsskiftaraskipan

Tað seinasta stigið at uppbyggja voltmetrið er samanbindingin av trýteljaranum gjøgnum stýriskipanina til digitalvoltmetrið. Stýriskipanin er uppbygd av kombinatoriskum rásum. Krøvini til stýriskipanina eru hesi:

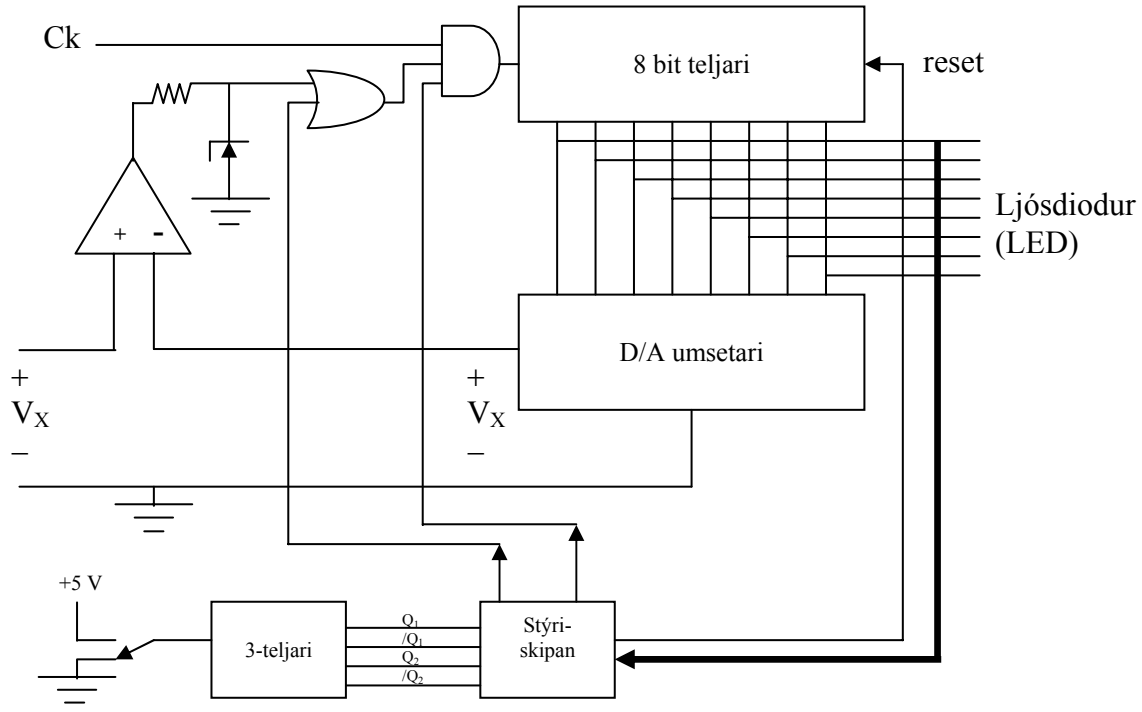
Støða 1: Voltmetrið er nulstillað, tá Q_1 $/Q_1$ Q_0 $/Q_0 = 0101$.
Hesi virði skulu stýra voltmetrinum, soleiðis at útgangurin á 8 bit teljaranum er 00000000, ella við øðrum orðum, teljarin verður nulstillaður.

Støða 2: Voltmetrið mátar ein spenning, tá Q_1 $/Q_1$ Q_0 $/Q_0 = 0110$.
Hesi virði stýra voltmetrinum soleiðis, at 8 bit teljarin ikki er nulstillaður, og at klokkupulsarnir koma ígjøgnum til teljaran, inntil komparatorsignalið, tá tað fær virðið 0, í hesi støðu avgerð, at klokkusignalið ikki longur kemur til teljarin.

Støða 3: Voltmetrið verður roynt svarandi til fullan spenning.
Hetta ber við sær, at Q_1 $/Q_1$ Q_0 $/Q_0 = 1001$, og skulu hesi virði stýra voltmetrinum soleiðis, at teljarin telur í hesum føri til útgangurin á 8 bit teljaranum er 11111111. Útgangssignalið á hesum

teljaranum skal so fáa teljaran at steðga, t.e. forða klokkusignalinum, at koma til inngangin á teljaranum.

Hetta verður gjørt við rásini sum víst í mynd 2.6.1.



Mynd 2.6.1

At svara áðrenn møtt verður í starvsstovuni í starvsstovuni:
Spurningur 14: Vís hvussu stýriskipanin kann verða uppbygd av t.d. tveimum "NAND-gate"um og einari "AND-gate" (onkur av teimum hevur eitt stórt tal av inngangum).

At svara í starvsstovuni:
Spurningur 15: Set stýriskipanina upp soleiðis, at tær trýggjar støðurnar virka.

2.7 Digitalvoltmetur við funktiónsskiftaraskipan til spenningsmáting, 0-stilling og 1-stilling av digitalútganginum.

Samlaða digitalvoltmeturskipanin verður nú roynd

At svara í starvsstovuni:
Spurningur 16: Máta í støðu 1 spenningin V og støðuna á ljósdiodunum fyri V_X = 0, 2, og 5 volt.

Spurningur 17: Máta í støðu 2 spenningin V og støðuna á ljósdiodunum fyri V_X = 0, 2, og 5 volt.

Spurningur 18: Máta í støðu 3 spenningin V og støðuna á ljósdiodunum fyri V_X = 0, 2, og 5 volt.

3. Starvsstovuútgerð

Til venjingina er henda starvstovuútgerð tøk:

- Digitalur royndarbonkur við innbygdum 5 volt spenningsgerða, klokkuspennings-gerða, digitalum 0/1-signal kontaktum, ljósdiodum til lesing av digitalsignalum, og haldarum til IC rásir ("Integrated Circuit chips").
- Ossilloskop við tveimum signalrásum
- Spenningsgerði við broytiligum spenningi
- Voltmetur (multimetur)
- Funktiónsspenningsgerði við sinus, trýkant og fýrkantspenningi við broytiligum frekvensi og amplitudu
- Tær IC rásir og mótstøður og kondensatorar, ið eru kravdar til venjingina
- Databløð og bøkur til IC rásirnar.

IV. CMI – KODING TIL LJÓSLEIÐARA DATASENDISKIPAN
STARVSTOVUVENJING

1. Inngangur
Venjingin snýr seg um greining av uppbygging og virkihátti í eini kodingsskipan, ið m.a. verður brúkt í optiskum transmissiónsskipanum. Skipanin er uppbygd av undireindum, sum hvør sær fyrst verður uppbygd og kannað. Síðan verða tær bundnar saman til eina samanhangandi transmissiónsskipan, hvørs transmissiónseginleikar verða kannaðir.

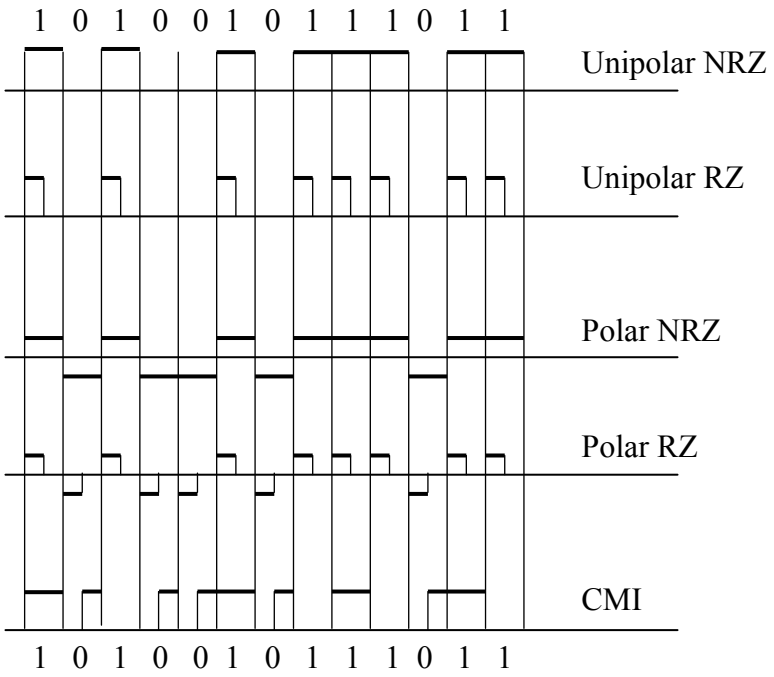
2. Kodiskipan - endamál og uppbyggjan
Í øllum digitalum tele- og datatransmissiónsskipanum, verða kodingsskipanir nýttar til tess at gera transmissiónina av information tryggast og best møguliga. Vanliga, tá information skal verða borin frá einum staði til annað, verður hetta gjørt við, at informatiónin verður gjørd um til eitt digitalt signal, ið kann vera binert, t.e. ein røð av "0"-um og "1"-um, sum verða send hvørt aftan á annað, t.e. sekventielt (serielt), á eini transmissiónslinju.

Verður soleiðis tann bineri framburðurin (representatiónin) av signalinum nýttur, býta vit tíðarásin upp í interval av ávísari longd T=1/f, har f verður nevndur klokkufrekvensurin. Í hvørjum av hesum intervallum senda vit eitt signalmynstur (spenningsmynstur), ið er ymiskt fyri "0" og "1", og sigur frá, hvørt av hesum verður sent. Hetta spenningsmynstur nevna vit eina kodu fyri transmissiónina.

Ein tann mest einfalda, og vit kunnu kanska siga grundleggjandi, kodingin er myndað av, at spenningurin í intervallinum er 0 volt svarandi til logiskt "0" og V volt svarandi til logiskt "1". Hesa koduna nevna vit ta bineru "unipolaru NRZ" koduna ("Non Return to Zero"). NRZ er víst í mynd 2.1 saman við øðrum kodum. Er spenningurin V volt bert helvtina av einum 1-intervalli verður kodan nevnd "unipolar RZ" ("Return to Zero").

Er logiskt "0" myndað av spenninginum –V/2, og "1" myndað av +V/2 , fáa vit tær tilsvarandi bipolaru ella bert polaru kodurnar.

Tað er ikki altíð, at transmissiónskodurnar eru so einfaldar við tað, at tað oftast er ynskt, at tær skulu uppfylla ymsar treytir fyri, at transmissiónin skal gerast so trygg og feilfrí sum gjørligt. Eginleikar í transmissiónini, ið hædd skal takast fyri, kunnu vera av ymiskum slag. Í koparkaðalum er soleiðis ynskt, at miðalvirðið av signalspenninginum skal vera so nær null, sum gjørligt er, av tí at transmissión av einum javnstreymi onga nyttu ger, men bert elvir til eitt orkutap. Tí er ynskt í hesum kaðalum, at tað kodaða signalið verður borið av einum spenningi, ið í meðal er null, t.e. eins ofta er positivur sum negativur. Tí verða polarar kodur valdar til hesa transmissión. Í glasfipurkaðalum er hetta ikki nakar trupulleiki við tað, at signalið her er ljós. Harafturímóti er í øllum digitalum transmissiónsskipanum avgerandi, at tað í móttøkuendanum er møguligt at fáa fatur í einum klokkusignali, ið ger tað møguligt at



Mynd 2.1

markera, nær tey digitalu signalmynstrini skulu verða avlisin. Hetta klokkusignalið kann sjálvsagt verða sent í serstakari sendikanal, men er tað ein dýrur máti, sum tí ikki verður nýttur.

Í veruligum kommunikatiónsskipanum verður klokkusignalið endurskapt úr sjálvum informatiónssignalinum, sum inniheldur ein frekvenskomposant (Fourier komposant) við sama frekvensi, sum klokkusignalið hevur, ella eitt heiltals multiplum av honum. Fyri at tryggja, at ein long røð av nullum ella eitt tølum í tí digitala signalinum ikki skal geva eitt langt tíðarbil har kaðalsignalið, tað veri seg í koparkaðali ella ljósleiðarakaðali, er konstant, og tað tí verður torført at endurskapa klokku-signalið, verður ein ella annar formur fyri koding nýttur, sum ger at signalið, sum sent verður, javnan skiftir við tíðini.

Í ljósleiðarasendiskipanum verður ofta tann sokallaða CMI kodan (coded mark inversion) brúkt. Hon fæst fram við at brúka hesar reglar (sí mynd 2.1):

- Logiskt “0” verður myndað í einum klokkuintervalli sum lágt signal í fyrru helvt av intervallinum og sum høgt signal í seinnu helvt av intervallinum, t.e. tað hendir eitt skift frá lágum til høgt signal í miðjuni av intervallinum. Vit kunnu sostatt siga at “0” verður umsett til at eita “01” við einum nýggjum klokkuintervalli, ið bert hevur hálva stødd av grundklokkuintervallinum.

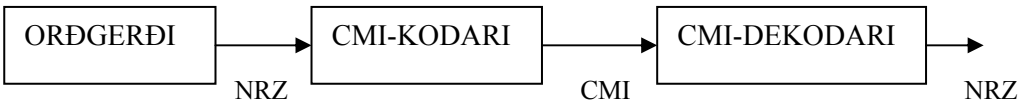
- Logiskt “1” verður myndað sum eitt støðugt signal í øllum data- klokkuintervallinum. Hetta skiftir millum at vera lágt og høgt aðruhvørja ferð logiskt ”1” kemur fyri. Vit kunnu sostatt siga at “1” er umsett til “00” ella “11” aðruhvørja ferð tað fyrikemur.

Tí er brúk fyri at gera eitt klokkusignal við dupultum klokkufrekvensi til tess at stýra CMI koduni. Hesa klokku nevna vit CMI-klokkuna.

Í venjingini verður ein CMI kodari og ein CMI dekodari, hóskandi til brúk í einari ljósleiðaraskipan, uppbygdur við IC rásum og royndur. Av tí at tað her snýr seg um at modulera signalið til eina ljósstrálu frá einum lasara, t.e. sløkkja og tendra hann, brúka vit lágan og høgan spenning frá IC rásunum til at mynda lágt og høgt niveau í CMI koduni, sum víst í mynd 2.1

Til tess at royna skipanina er brúk fyri einum digitalum inngangssignali, ið er eitt tilvildarligt býti av "0" og "1" á tíðarásinum. Best hevði verið at havt ein tilvildarligan orðgerða ella bitgerða til hetta endamál; men til hesa venjingina byggja vit ein orðgerða við einum føstum 8 ella 16 bit orði, ið verður endurtikið periodiskt, og sum vit kunnu stilla eftir ynski.

Yvirlitsuppsetingin av skipanini sær út sum víst í mynd 2.2. Úr orðgerðanum kemur ein røð av bittum í NRZ kodu, sum verður umgjørdur til CMI kodu í CMI-kodaranum. Hetta CMI signalið er tað signalið, ið vanliga verður sent gjøgnum ljósleiðaran, sum kortini ikki er við í hesi venjingini. Í móttøkuendanum verður CMI signalið móttikið aftur, og síðan umger CMI-dekodarin hesa koduna aftur til NRZ kodu.



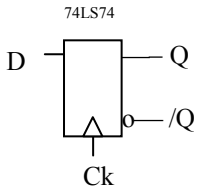
Mynd 2.2

3. Klokkur

Dataklokkan er grundklokkusignalið, ið stýrir datasignalinum. Síðan hava vit eisini brúk fyri einum CMI-klokkusignali við dupult so stórum frekvensi, sum dataklokkan hevur. Eitt slíkt signal kann verða gjørt við ólineerum elektronikki og liggur uttan fyri evni í hesi venjingini. Vit skulu heldur ganga hinvegin og byrja við eini CMI-klokku. Við eini flip-flop IC-rás skapa vit eitt dataklokkusignal við hálvum CMI-klokku frekvensi. Vit velja ein D flip-flop 74LS74(mynd 3.1).

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 1: Ger eitt diagramm av klokkusignalgerðanum og vís, hvar dataklokka og CMI-klokka eru.

At svara í starvsstovuni:
Spurningur 2: Bygg klokkusignalgerðan upp og royn hann.



D	Q	/Q
0	0	1
1	1	0

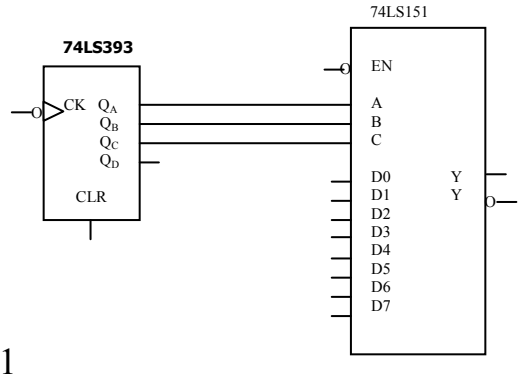
Mynd 3.1

4. Orðgerði

Í hesi venjing hevði verið best at brúkt ein orðgerða, ið ger tilvildarlig orð, til at royna CMI kodaran og dekodaran við. Hann er ikki tøkur. Í staðin fyri vilja vit byggja ein orðgerða, ið kann gera eina fyriskrivaða røð av bittum, ið síðan verður endurtikin periodiskt. Í byrjanini velja vit 8 bit, sum so eitt í senn við hjálp av einum multipleksara 74LS151 verða send út á útgangin Y. Adressuinngangirnir ABC fáa signal frá binera teljaranum 74LS393 sum víst á mynd 4.1. Orðið, ið verður sent út á Y-útganginum er D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7, ið er sett til logiskt ”0” ella logiskt ”1”, svarandi til orðið, ið vit ynskja.

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 3: Hvussu kunnu vit broyta orðgerðan við at brúka enable inngangin á multipleksaranum , soleiðis at 8 bit røðin, sum vit hava stillað við givnum virðum verður eftirfylgd av 8 nullum, og síðan endurtikið periodiskt.

At svara í starvsstovuni:
Spurningur 4: Set 8 bit orðgerðan upp. Ger broytingina sambært sp.3. Royn orðgerðan, áðrenn og aftan á broytingina.



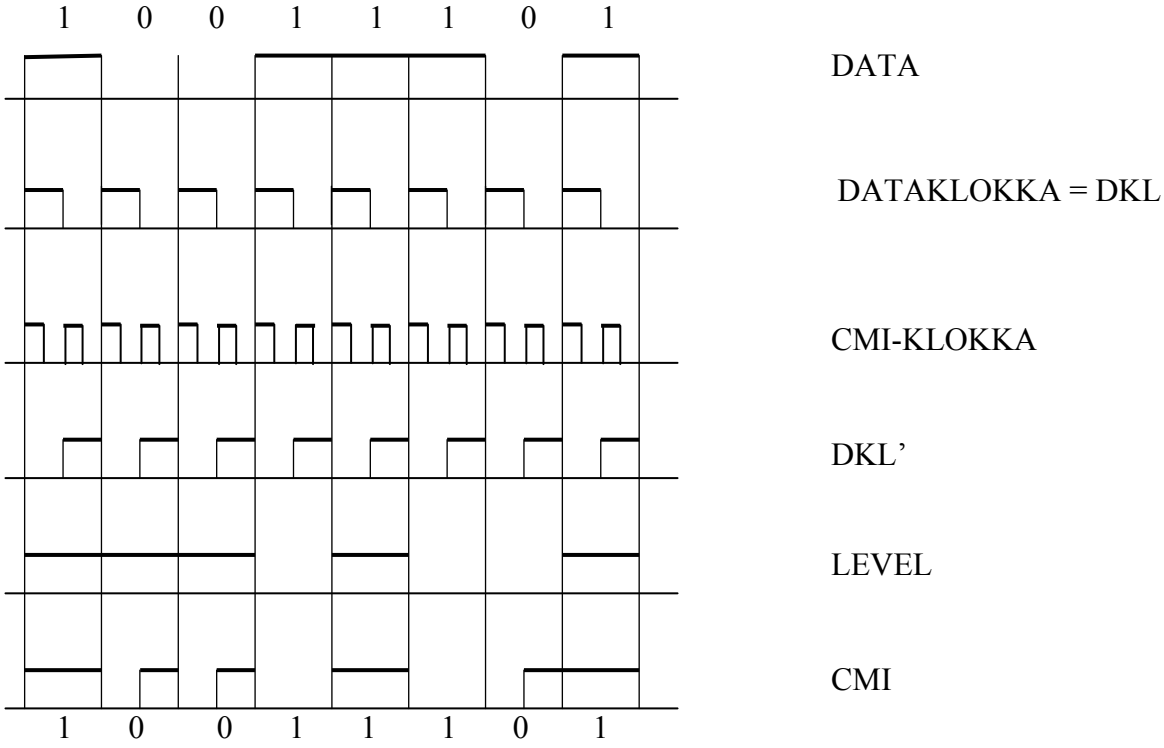
Mynd 4.1

5. CMI-kodari

Sum tað gongur fram av frágreiðingini í parti 2 og mynd 5.1, ger CMI kodarin brúk av einum klokkufrekvensi, sum er dupult so stórur sum dataklokkufrekvensurin.

Nú er so spurningurin, hvørjir inngangsvariablar stýra, hvørjum virði 0 ella 1, ið CMI útgangurin skal hava í hvørjum CMI-klokkuintervalli.

Givið er, at datasignalið, ið vit nevna DATA, má vera inngangsvariabul. Vit síggja eisini, at CMI signalið, svarandi til DATA = 0, skiftir í miðjum intervalli. Hetta ger dataklokkan eisini. Tí má dataklokkusignalið “DKL” vera ein hóskandi inngangsvariabul.



Mynd 5.1

CMI signalið svarandi til DATA=1 er konstant í tveimum CMI-klokkuintervallum, men skiftir virði til 0 og 1 aðruhvørja ferð 2 CMI klokkusignal hava verið. Tí mugu vit hava ein variabul, lat okkum nevna hann LEVEL, sum stýrir CMI signalvirðinum í "1" intervallum, og skiftir virði hvørja ferð eitt DATA=1 kemur inn, men heldur virði tá DATA=0. Level er hinvegin ikki eitt útifrá komandi signal, men má verða gjørt í skipanini. Av tí at LEVEL bert broytist, tá DATA hevur verið tvær ferðir 1, tá ein CMI klokkupulsur kom, má tann digitala maskinan, sum skapar LEVEL hava 4 støður svarandi til 2 støðuvariablar (2 flip-flop).

At svara áðrenn møtt verður í starvsstovuni:
Spurningur 5: Vís, at útgangssignalið CMI = DATA'•DATAKL' + DATA•LEVEL
(• er brúkt fyri "AND"). Allar støður eru vístar á mynd 5.1.

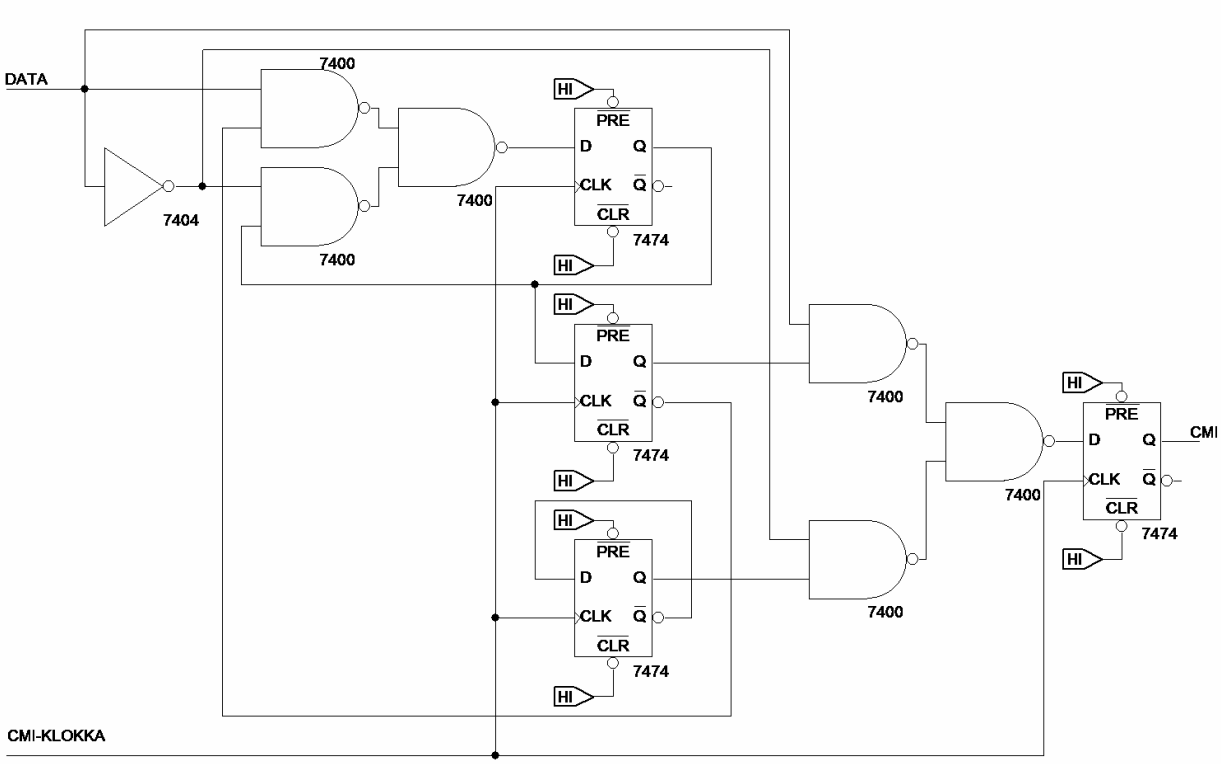
Spurningur 6: Vís, at tann við CMI- klokkuna synkrona digitala maskinan í mynd 5.2 gevur LEVEL signalið. Hetta verður gjørt við at

- finna excitatiónslíkningarnar
- skriva yvirgangs/útgangstalvu upp
- skriva støðu/útgangstalvu upp
- definera støðurnar
- tekna støðudiagramm
- vís á hvar í mynd 5.2 LEVEL signalið er.

Spurningur 7: Vís, at ein digital maskina við bert einum D flip-flop, ið er synkron við dataklokkuna DKL eisini kann geva LEVEL signalið. Konstruera hesa maskinuna við at

- definera støðurnar
- tekna støðudiagramm
- skriva støðu/útgangstalvu upp
- skriva yvirgangs/útgangstalvu upp
- finna excitatiónslíkningarnar
- tekna rásina (diagrammið) upp.

At svara í starvsstovuni:
Spurningur 8: Bygg CMI kodaran við at brúka aðra av loysnunum frá sp.6 ella 7.



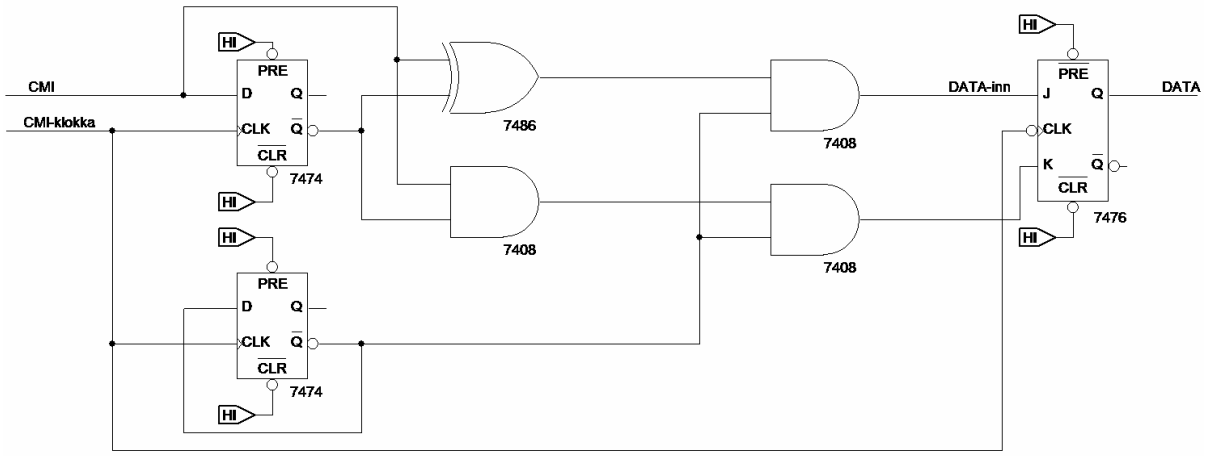
Mynd 5.2 CMI – kodari

6. CMI - dekodari

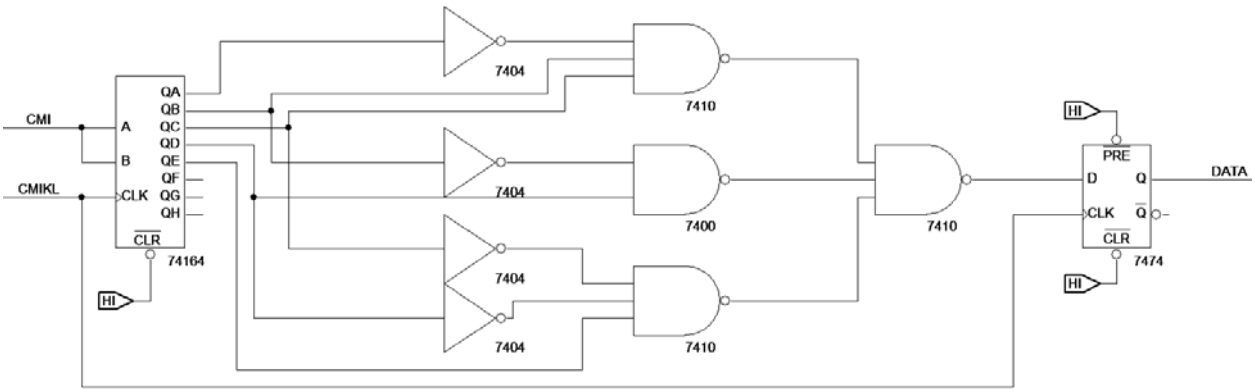
Ein dekodari er ein digital maskina, sum broytir CMI koduna til eitt datasignal (tað upprunaliga) við NRZ kodu sambært

CMI koda	DATA (NRZ-koda)
01	00
00	11
11	11

Í venjingini ganga vit út frá aðrari av teimum givnu rásunum fyri ein CMI dekodara, sum mynd 6.1 ella mynd 6.2 vísir (uppseting í mynd 6.2 er lættari at fáa at virka).



Mynd 6.1 CMI – dekodari, bygdur við flip-floppum



Mynd 6.2 CMI – dekodari bygdur við skiftiregisturi

At svara áðrenn møtt verður í starvsstovuni, svarandi til mynd 6.1:

Spurningur 9: Finn exitatiónslíkningarnar.

Spurningur 10: Finn yvirgangslíkningarnar (transitiónslíkningarnar) fyri flip-flopparnar.

Spurningur 11: Skriva yvirgangstalvuna (transitiónstalvuna) upp.

Spurningur 12: Navngev støðurnar, og skriva støðutalvuna upp.

Spurningur 13: Tekna støðudiagramm.

Spurningur 14: Tekna eina tíðarmynd, har CMI datasignal og datasignal, og eitt passandi tal av millumsignalum eru tikin við.

Spurningur 15: Vís, at fyri at fáa hesa uppseting at virka krevst synkronisering av dekodaranum til røttu hálvperioduna av dataintervallinum.

At svara áðrenn møtt verður í starvsstovuni, svarandi til mynd 6.2:
Spurningur 16: Skriva sannleikatalvuna upp fyri kombinatorisku rásina DATAinn sum funktión av QA,QB,QC,QD og QE útgangirnar í skiftiregistrinum svarandi til CMI dekoding. Vís at hendan funktiónin kann realiserast við vístu logisku rásini. Vís at útgangsvirði DATA á CMI dekodaranum eru somu data sum inngangsvirði DATA í CMI kodaran.

At svara í starvsstovuni:
Spurningur 17: Set rásina av CMI dekodaranum saman sum í mynd 6.1 ella mynd 6.2 , og royn hana.

7. CMI kodara – dekodara skipan

At svara í starvsstovuni:
Spurningur 18: Fyri at kunna fáa CMI kodara og CMI dekodara at arbeiða saman, er neyðugt at gera eitt synkroniseningssignal sum nulstillar teir samstundis, t.d. tá teljarin, ið stýrir bitsekvensinum hevur útgangin 1111. Ger hesa rásina, um uppsetingin í mynd 6.1 verður brúkt. Synkronisering er ikki neyðug til rásini í mynd 6.2.

Spurningur 19: Samanbind allar lutskipaninar og royn samlaðu skipanina við at samanbera bitsamansetingina frá orðgerðanum, og tað CMI dekodaranum gjørda signalið.

Spurningur 20: Hví skulu D-flip-floppar vera settir í útgangin av CMI kodaranum og í útgangin av CMI dekodaranum í mynd 6.2.

8. Fyrireiking

Áðrenn venjingina verður umframt hesa leiðbeining lisið í lærubókini av J.F.Wakerly:"Digital Design, Principles and practices":

- 5.6 Multiplexers
- 7.3 Clocked synchronous state-machine analysis
- 7.4 Clocked synchronous state-machine design
- 8.4 Counters
- 8.5 Shift registers

9. Starvsstovuútgerð

Til venjingina er henda starvstovuútgerð tøk:

- Digitalur royndarbonkur við innbygdum 5 volt spenningsgerða, klokkuspennings-gerða, digitalum 0/1-signal kontaktum, ljósdiodum til lesing av digitalsignalum, og haldarum til IC rásir ("Integrated Circuit chips").
- Monteringspláta ("breadboard") til montering av komponentum
- Oscilloskop við tveimum signalrásum
- Voltmetur (multimetur)
- Funktiónsspenningsgerði við sinus, trýkant og fýrkantspenningi við broytiligum frekvensi og amplitudu
- Tær IC rásir og aðrir komponentar, ið eru kravd til venjingina
- Databløð og bøkur til IC rásirnar.

V. Databløð (úrtøk)

5400/DM5400/DM7400 Quad 2-Input NAND Gates

National Semiconductor

June 1989

5400/DM5400/DM7400
Quad 2-Input NAND Gates

General Description

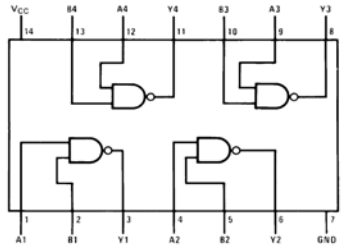
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5400) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6613–1

Order Number 5400DMQB, 5400FMQB, DM5400J, DM5400W or DM7400N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

5402/DM5402/DM7402 Quad 2-Input NOR Gates

National Semiconductor

June 1989

5402/DM5402/DM7402
Quad 2-Input NOR Gates

General Description

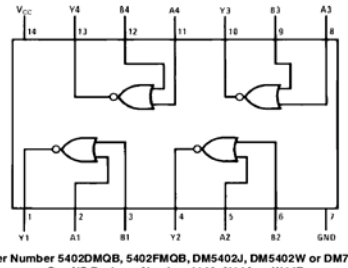
This device contains four independent gates each of which performs the logic NOR function.

Features

- Alternate Military/Areospace device (5402) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6492–1

Order Number 5402DMQB, 5402FMQB, DM5402J, DM5402W or DM7402N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{A + B}$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

DM7404 Hex Inverting Gates

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7404
Hex Inverting Gates

General Description

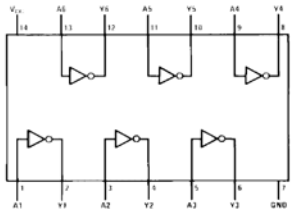
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{A}$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

DM7408 Quad 2-Input AND Gates

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised February 2000

DM7408
Quad 2-Input AND Gates

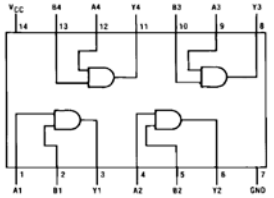
General Description

This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

National Semiconductor

June 1989

5410/DM5410/DM7410 Triple 3-Input NAND Gates

General Description

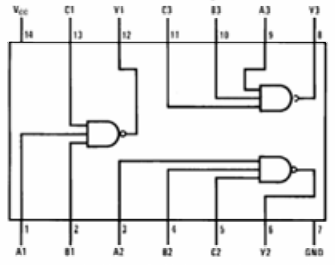
This device contains three independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5410) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6500–1

Order Number 5410DMQB, 5410FMQB, DM5410J, DM5410W or DM7410N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

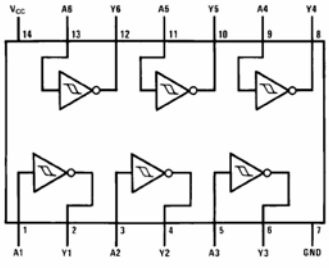
DM5414/DM7414 Hex Inverter with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6503–1

Order Number DM5414J, DM5414W or DM7414N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

5420/DM5420/DM7420 Dual 4-Input NAND Gates

General Description

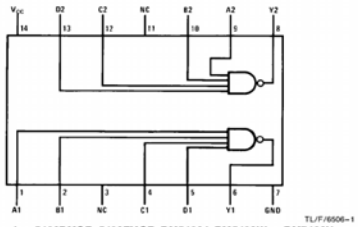
This device contains two independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (5420) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6506–1

Order Number 5420DMQB, 5420FMQB, DM5420J, DM5420W or DM7420N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

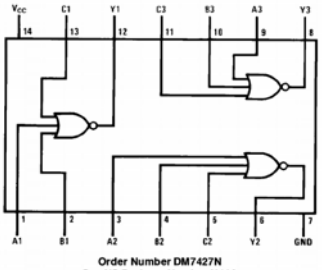
DM7427 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6509–1

Order Number DM7427N
See NS Package Number N14A

Function Table

$Y = \overline{A + B + C}$

Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

5430/DM5430/DM7430
8-Input NAND Gate

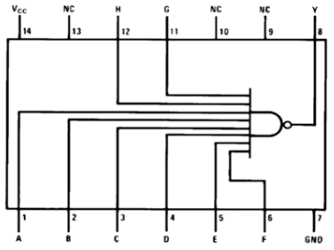
General Description

This device contains a single gate which performs the logic NAND function.

- Alternate Military/Aerospace device (5430) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6610–1

Order Number 5430DMBQ, 5430FMQB, DM5430J, DM5430W or DM7430N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = \overline{ABCDEFGH}$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

5432/DM5432/DM7432
Quad 2-Input OR Gates

General Description

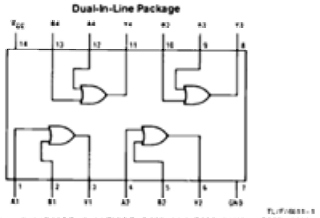
This device contains four independent gates each of which performs the logic OR function.

Features

- Alternate Military/Aerospace device (5432) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 5432DMQB, 5432FMQB, DM5432J, DM5432W or DM7432N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised July 2001

DM7474
Dual Positive-Edge-Triggered D-Type Flip-Flops with Preset, Clear and Complementary Outputs

General Description

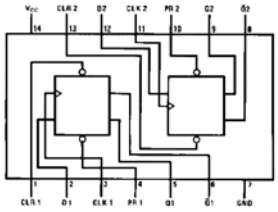
This device contains two independent positive-edge-triggered D-type flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM7474M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7474N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going transition of the clock.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

 DS006526

National Semiconductor

June 1989

5476/DM5476/DM7476
Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

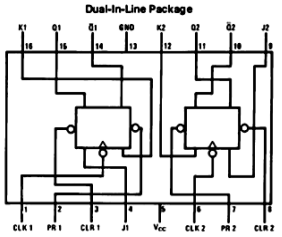
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (5476) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6528–1

Order Number 5476DMQB, 5476FMQB,
DM5476J, DM5476W or DM7476N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓⊔	L	L	Q_0	$\overline{Q}_0$
H	H	⊓⊔	H	L	H	L
H	H	⊓⊔	L	H	L	H
H	H	⊓⊔	H	H	Toggle	

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
⊓⊔ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.
* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

5486/DM5486/DM7486
Quad 2-Input Exclusive-OR Gates

General Description

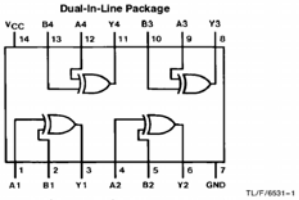
This device contains four independent gates each of which performs the logic exclusive-OR function.

Features

- Alternate Military/Aerospace device (5486) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6531–1

Order Number 5486DMQB, 5486FMQB, DM5486J, DM5486W or DM7486N
See NS Package Number J14A, N14A or W14B

Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

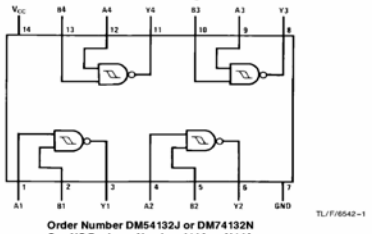
DM54132/DM74132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Connection Diagram

Dual-In-Line Package



TL/F/6542–1

Order Number DM54132J or DM74132N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

54150/DM54150/DM74150,
54151A/DM54151A/DM74151A
Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

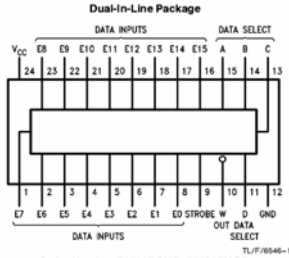
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
  - 150 11 ns
  - 151A 9 ns
- Typical power dissipation
  - 150 200 mW
  - 151A 135 mW
- Alternate Military/Aerospace device (54150, 54151A) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

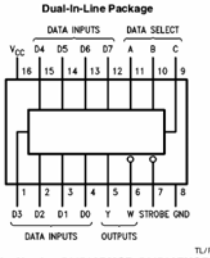
Dual-In-Line Package



TL/F/6546–1

Order Number 54150DQMB, 54150FMQB, DM54150J or DM74150N
See NS Package Number J24A, N24A or W24C

Dual-In-Line Package



TL/F/6546–2

Order Number 54151ADMQB, 54151AFMQB, DM54151AJ, DM54151AW or DM74151AN
See NS Package Number J16A, N16E or W16A

RRD-B30M105/Printed in U. S. A.

FAIRCHILD SEMICONDUCTOR TM

September 1986
Revised July 2001

DM74164
8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A LOW logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the LOW level at the next clock pulse, thus providing complete control over incoming data. A HIGH logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the LOW-to-HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

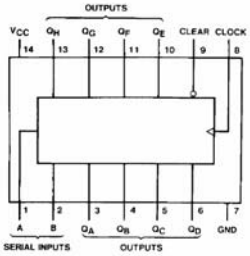
Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74164	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

 DS006552

National Semiconductor

June 1989

DM74LS393 Dual 4-Bit Binary Counter

General Description

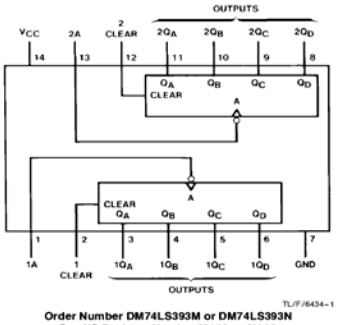
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count freqency is available for system-timing signals.

Features

- Dual version of the popular 'LS93
- 'LS393 dual 4-bit binary counter with individual clocks
- Direct clear for each 4-bit counter
- Dual 4-bit versions can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency 35 MHz
- Buffered outputs reduce possibility of collector commutation

Connection Diagram

Dual-In-Line Package



TL/F/6434–1

Order Number DM74LS393M or DM74LS393N
See NS Package Number M14A or N14A

Function Table

Count Sequence (Each Counter)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Clear	7V
A	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM74LS393 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	MHz
t_W	Pulse Width (Note 7)	A	20			ns
		Clear High	20			
t_{REL}	Clear Release Time (Notes 3 & 7)		25 ↓			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	µA
			A			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.
Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.
Note 3: The symbol (↓) indicates that the falling edge of the clear pulse is used for reference.
Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.
Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 6: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
Note 7: T_A = 25°C, and V_{CC} = 5V.

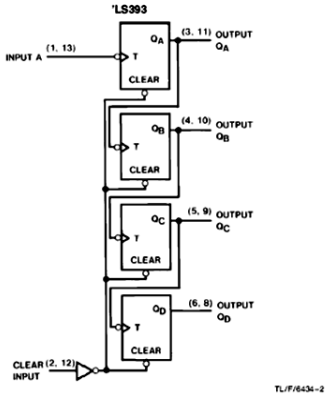
 TL/F/6434

RRD-B30M105/Printed in U. S. A.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ C_L = 15 pF Min	C_L = 15 pF Max	C_L = 50 pF Min	C_L = 50 pF Max	Units
f_{MAX}	Maximum Clock Frequency	A to Q_A	25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		39		45	ns

Logic Diagram



TL/F/6434–2

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised February 1999

DM74LS191
Synchronous 4-Bit Up/Down Counter with Mode Control

General Description

The DM74LS191 circuit is a synchronous, reversible, up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a LOW-to-HIGH level transition of the clock input, if the enable input is LOW. A HIGH at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is HIGH. The direction of the count is determined by the level of the down/up input. When LOW, the counter counts up and when HIGH, it counts down.

The counter is fully programmable; that is, the outputs may be preset to either level by placing a LOW on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Ordering Code:

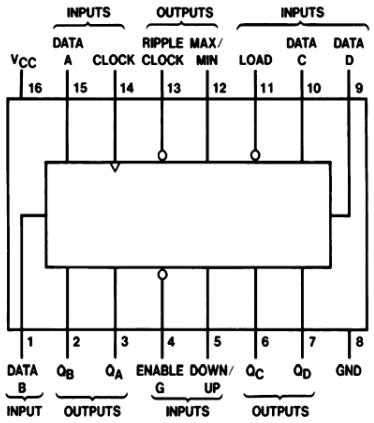
Order Number	Package Number	Package Description
DM74LS191M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
DM74LS191N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

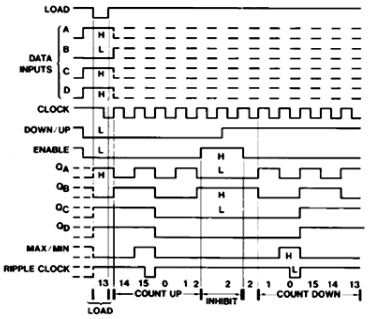
 DS006405.prf

www.fairchildsemi.com

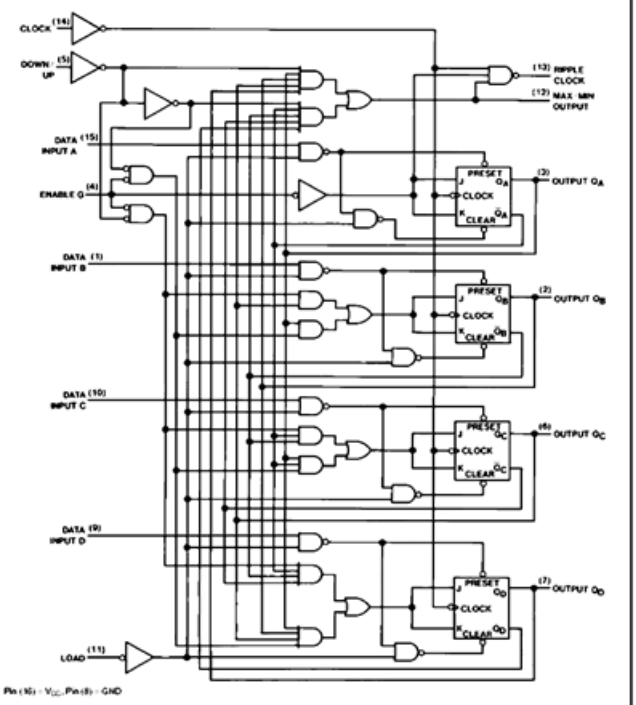
Connection Diagram



Timing Diagram



Logic Diagram



National Semiconductor

January 1995

DAC0808/DAC0807/DAC0806 8-Bit D/A Converters

General Description

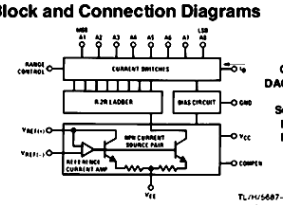
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current setting time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

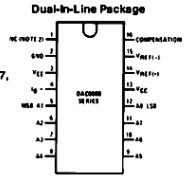
- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



Order Number DAC0808, DAC0807, or DAC0806
See NS Package Number J16A, M16A or N16A

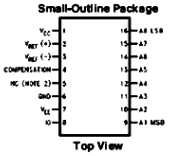
Dual-In-Line Package



TL/H/5687-2

TL/H/5687-1

Small-Outline Package



Top View

TL/H/5687-13

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
7-bit	0°C ≤ T_A ≤ +75°C	DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7	DAC0807LCM
6-bit	0°C ≤ T_A ≤ +75°C	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM
				DAC0808LCN	MC1408P8	DAC0808LCM

*Note. Devices may be ordered by using either order number.

RRD-B30M115/Printed in U.S.A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
DAC0808LC Series	0 ≤ T_A ≤ +75°C

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 5)				±0.39	%
	DAC0806LC (LM1408-6), (Note 5)				±0.78	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C (Note 6), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TC_{I_O}	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance (Note 2)	$E_r \leq$ 0.19%, T_A = 25°C				
	V_{EE} = −5V, I_{REF} = 1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −16.5V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application

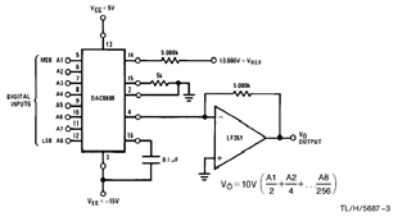
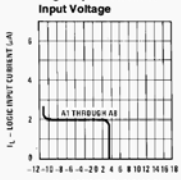


FIGURE 1. +10V Output Digital to Analog Converter (Note 7)

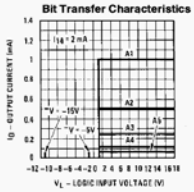
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

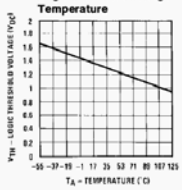
Logic Input Current vs Input Voltage



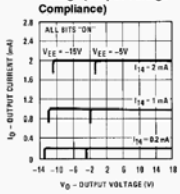
Bit Transfer Characteristics



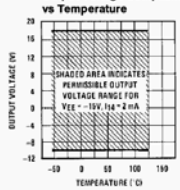
Logic Threshold Voltage vs Temperature



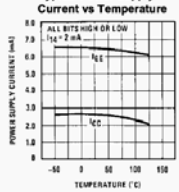
Output Current vs Output Voltage (Output Voltage Compliance)



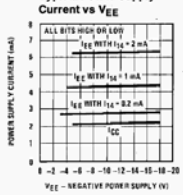
Output Voltage Compliance vs Temperature



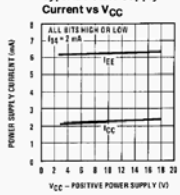
Typical Power Supply Current vs Temperature



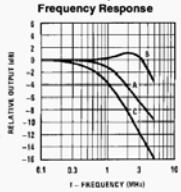
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

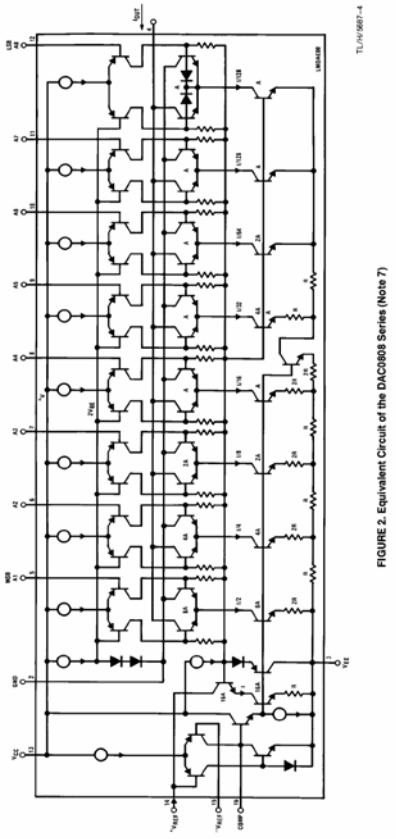
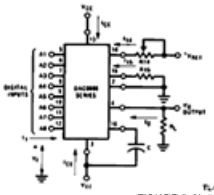


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 7)

Test Circuits



V_I and I_I apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

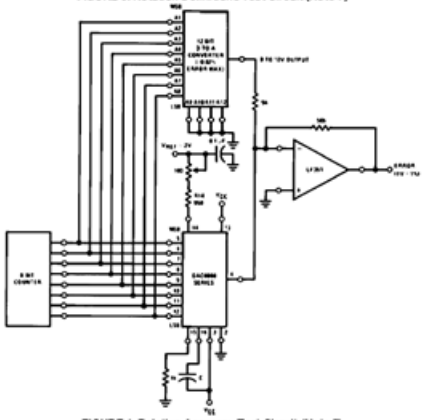
where $K = \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

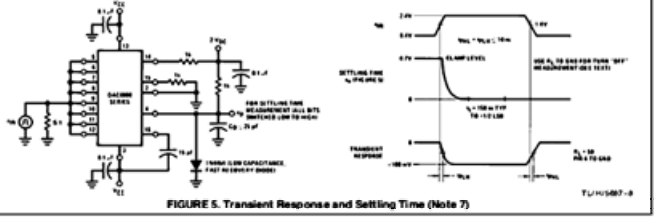
TL/H/5687–6

FIGURE 3. Notation Definitions Test Circuit (Note 7)



TL/H/5687–7

FIGURE 4. Relative Accuracy Test Circuit (Note 7)



TL/H/5687–8

FIGURE 5. Transient Response and Settling Time (Note 7)

Test Circuits (Continued)

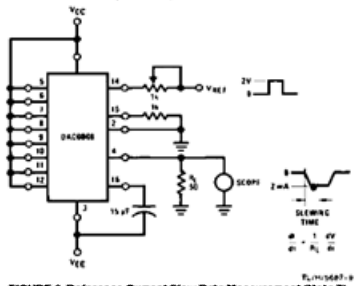


FIGURE 6. Reference Current Slew Rate Measurement (Note 7)

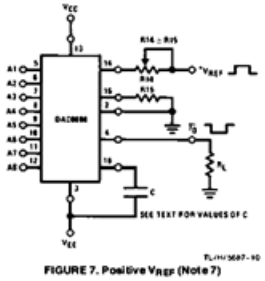


FIGURE 7. Positive V_{REF} (Note 7)

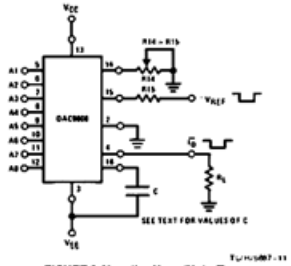


FIGURE 8. Negative V_{REF} (Note 7)

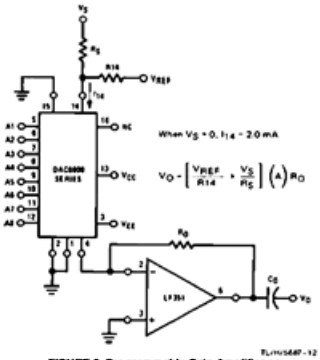


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 7)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

Application Hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.55 to 0.4V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±½ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±½ of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±½ LSB, for 8-bit accuracy, and 100 ns to ½ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

October 2002

ADC0808/ADC0809
8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

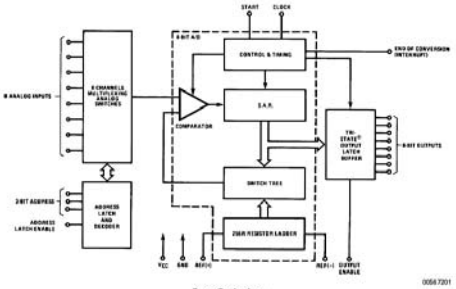
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

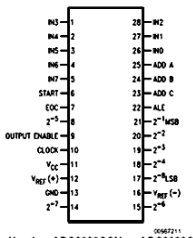
Block Diagram



See Ordering Information

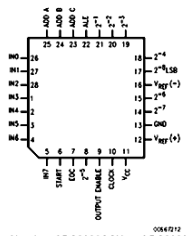
Connection Diagrams

Dual-In-Line Package



Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C	
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

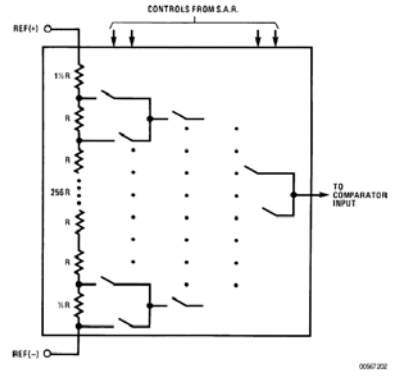


FIGURE 1. Resistor Ladder and Switch Tree

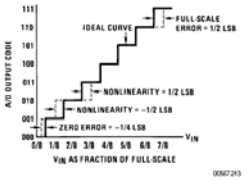


FIGURE 2. 3-Bit A/D Transfer Curve

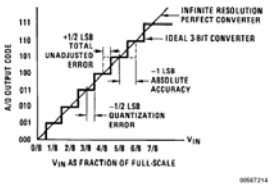


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

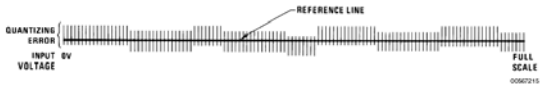


FIGURE 4. Typical Error Curve

National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

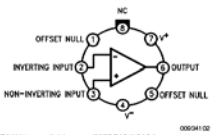
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0˚C to +70˚C temperature range, instead of −55˚C to +125˚C.

Features

Connection Diagrams

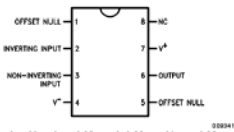
Metal Can Package



Note 1: LM741H is available per JM38510/10101

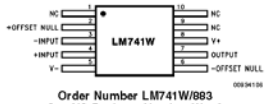
Order Number LM741H, LM741H/883 (Note 1), **LM741AH/883 or LM741CH**
See NS Package Number H08C

Dual-In-Line or S.O. Package



Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

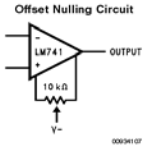
Ceramic Flatpak



Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



 DS009341

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55˚C to +125˚C	−55˚C to +125˚C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Junction Temperature	150˚C	150˚C	100˚C
Soldering Information			
N-Package (10 seconds)	260˚C	260˚C	260˚C
J- or H-Package (10 seconds)	300˚C	300˚C	300˚C
M-Package			
Vapor Phase (60 seconds)	215˚C	215˚C	215˚C
Infrared (15 seconds)	215˚C	215˚C	215˚C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A Min	LM741A Typ	LM741A Max	LM741 Min	LM741 Typ	LM741 Max	LM741C Min	LM741C Typ	LM741C Max	Units
Input Offset Voltage	$T_A = 25˚C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/˚C
Input Offset Voltage Adjustment Range	$T_A = 25˚C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25˚C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/˚C
Input Bias Current	$T_A = 25˚C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25˚C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25˚C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit	$T_A = 25°C$	10	25	35		25			25		mA
Current	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
Ratio	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

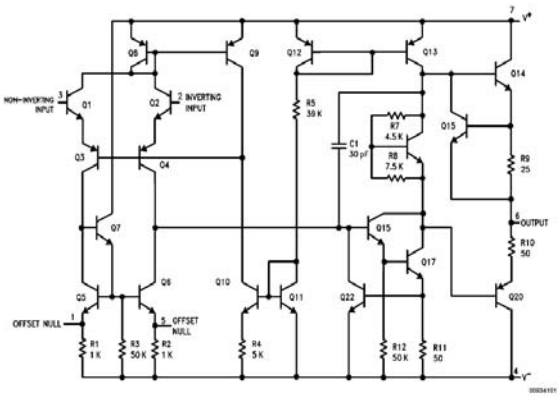
Note 5: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1747
MC1747C

2

(Dual MC1741)
Internally Compensated, High Performance Operational Amplifiers

(DUAL MC1741)
DUAL OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC1747 and MC1747C were designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the µA747 and µA747C respectively.

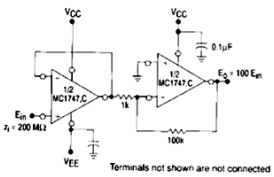
- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up
- Offset Voltage Null Capability

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

P2 SUFFIX
PLASTIC PACKAGE
CASE 646

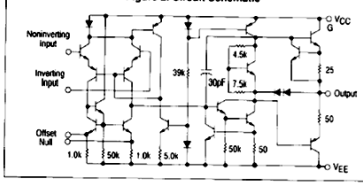
L SUFFIX
CERAMIC PACKAGE
CASE 632

Figure 1. High-Impedance, High-Gain Inverting Amplifier

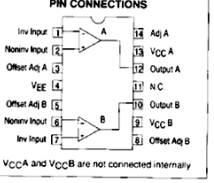


Terminals not shown are not connected

Figure 2. Circuit Schematic



PIN CONNECTIONS



VCCA and VCCB are not connected internally

ORDERING INFORMATION

Device	Temperature Range	Package
MC1747L	−55° to +125°C	Ceramic DIP
MC1747CD	0° to +70°C	SO-14
MC1747CL		Ceramic DIP
MC1747CP2		Plastic DIP

National Semiconductor

November 1994

LM747
Dual Operational Amplifier

General Description

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

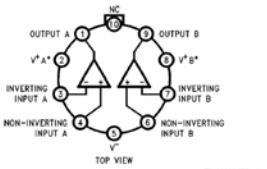
The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Balanced offset null

Connection Diagrams

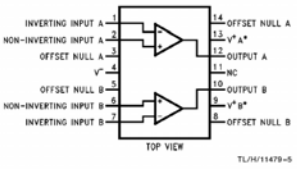
Metal Can Package



TL/H/11479–4

Order Number LM747H
See NS Package Number H10C

Dual-In-Line Package



TL/H/11479–5

Order Number LM747CN or LM747EN
See NS Package Number N14A

*V+ A and V+ B are internally connected.

RRD-B30M115/Printed in U. S. A.